HIGH EFFICIENCY ONE, TWO, AND FOUR WATT CLASS B FET POWER AMPLIFIERS

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ABSTRACT

A family of X-band amplifiers utilizing the higher efficiency of class B operation has been designed and fabricated. This paper describes the circuitry and performance of 1 watt single-ended, 2 watt push-pull, and 4 watt dual push-pull amplifiers having typical power-added efficiencies of 45%, 40%, and 35%, respectively, in a 1 GHz bandwidth, with associated gains of 5.8 dB, 5.4 dB, and 5.0 dB. Additional data is given for fifteen each of the 1 watt and 2 watt units to show the consistency of their performance.

INTRODUCTION

Class B operation of microwave FETs leads to an increase in efficiency and thereby substantial reductions of both dc power and heat dissipation.[1] In addition to power output and efficiency data, this paper addresses the large signal non-linear effects of AM to PM conversion, second harmonic generation, intermodulation products, and phase non-linearity characteristics for a group of fifteen 1 watt single-ended amplifiers and a group of fifteen 2 watt push-pull amplifiers.[2]

Because the transconductance of the FETs used is constant over most of the gate-to-source voltage range but decreases close to pinch-off, the amplifiers were biased to a quiescent drain current value of $I_{DQ} \simeq 10\%\ I_{DSS}$ for reasonable gain, without greatly lowering efficiency. Hence these amplifiers do not operate purely class B, but to a close approximation; the FET conduction angle is not much larger than 180°.

Before discussing the measured results, attention will be focused on the FETs for class B amplification and on circuit design techniques and topologies.

FET DEVICE CHARACTERISTICS

The device in all the amplifiers was the Fujitsu FLK 102XV. The FLK 102 was used in chip form for size considerations and to allow the input matching scheme described next. The 2400 μm periphery device employs plated-through source vias for bondless source grounding and good heat-sinking. Eight individual FETs were characterized at 9.7 GHz at both small signal and rated power levels using loss-corrected tuner measurements. The average chip output power, gain, and power-added efficiency were 30.8 dBm, 6.0 dB, and 48%. Bias conditions were V_D = 8.5v, I_{DQ} = 40 ma ($\simeq$ 10% I_{DSS}) and $V_G \simeq -2.1$v.

CIRCUIT DESIGN

A major requirement of this effort was flatness of both output power and efficiency in the 9.2-10.2 GHz band. Thus the tradeoff of an increased number of tuning elements for flat response versus the additional loss they would introduce was a major concern. The averaged small signal input model of the FLK 102 at 10% I_{DSS} quiescent bias and conjugate output power match conditions was 2.5 ohms in series with 1.8 pf, giving an input Q of 3.7 at 9.7 GHz. Load pull tests yielded a Q of 1.2 for the equivalent output circuit. A double-tuned input matching network was thus necessary for flatness, while only a single-tuned section was employed at the drain to reduce output power losses.

The available direct access to the gates of the FETs made the following input matching network possible: Two bond wires were connected from the outboard gate pads to RF ground through 5 pf blocking chip capacitors, Figure 1a, resulting in an immediate parallel resonance of the input capacitance, thereby up-transforming the input resistance. A series L/shunt C section then achieved the rest of the transformation with good flatness. Only a series L/shunt C was needed on the drain because of the much lower Q of the FET output.

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Critical in the input matching was the necessity of a high Q gate shunt-resonating circuit. The short (~.012") shunt bondwire inductances were assumed to have low series resistance and so were the 5 pf blocking caps. First results on the 4 watt amplifier showed good output power but low gain and power-added efficiency, implying high input losses. These losses naturally have their greatest effect at the lowest impedance point of the input, i.e., the FET. This led to an investigation of the blocking caps and the discovery, through DeLoach resonance tests of the 5 pf chips, that the equivalent series resistance of these high dielectric constant (ε_R >400) capacitors was 1.3 ohms, giving an extremely low Q_{cap} = 2.5. Needless to say, this caused significant gain degradation at the 2.5Ω impedance level of the FET input. Lower ε_R (≃110) chip caps were obtained and tested to have less than .2 ohms series resistance, and they restored the gain and efficiency of the gate-shunt-resonated FET nearly to individual chip performance values.

1, 2, and 4 WATT AMPLIFIER TOPOLOGIES

1 Watt Single-Ended

The 1 watt single-ended amplifier used one FLK 102XV, with matching described as above. The L-C sections at the input and output were realized using series lengths of transmission line and shunt open stubs. High impedance shorted quarter-wavelength stubs delivered drain bias; at the second harmonic of the amplified signal these stubs act as half-wavelength shorts to the drain to give a harmonic tuning effect. Experiments had shown an increase in output power of up to 5% from this effect.

2 Watt Push-Pull

To obtain 2 watts output power it was necessary to combine two of the FETs. This was done in a push-pull manner, Figure 1b, using novel 0°-180° hybrid splitters, which are not shown. Since the FETs in this case were driven antiphase, the virtual ground symmetry between them permitted the combination of some matching circuitry. First, the separate gate-resonating inductance bonds on the common side of the two FETs were replaced by one FET-to-FET gate bond, eliminating two of the dc-blocking capacitors. The gates of the FET pair were thus dc-common. Also the input and output shunt-open tuning stubs were replaced by capacitor chips bonded between each side of the antiphase I/O transmission lines.

4 Watt Dual Push-Pull

A 4 watt dual push-pull topology was obtained by paralleling a pair of the 2 watt amplifiers through X-band Wilkinson power splitters having .2 dB dissipative loss each.

PERFORMANCE RESULTS

The measured results are described in two parts:

1) There is a direct comparison of optimal 1, 2, and 4 watt individual amplifiers, each of which was made using high - Q gate - blocking capacitors. The drain voltage of 9 v was used to achieve an output of slightly more than 4 watts needed from the dual push-pull unit, per the requirements of the relevant NRL program, and the 1 and 2 watt individual units were biased accordingly.

2) The performance of 15-lots of the 1 watt and 2 watt amplifiers is given to show their repeatability and the consistency of the design. All 30 of the amplifiers initially contained low-Q gate blocking capacitors; after discovering the impact of their lossiness, high-Q capacitors were retrofitted in the 15 1 watt amplifiers. Since, as explained, the 2 watt push-pull topology inherently eliminates two of these capacitors, the smaller gain/efficiency improvement anticipated by installing high-Q ones in those units was judged unecessary to meet program requirements. Also, the drain voltage was set at 8 v for all 30 amplifiers because the AFWAL program called for power levels equal to or slightly less than 1 and 2 watts.

1, 2, and 4 Watt Amplifier Comparison

Figure 2 compares output power and power-added efficiency versus frequency for 1, 2, and 4 watt amplifiers. Roughly, the output power doubles, the gain drops about .4 dB and the efficiency decreases 5% at each upward step in the amplifier family. This is attributable mainly to losses in the Wilkinson and/or 0^o-180^o hybrids needed for power doubling. The dual push-pull amp had output power of 4.0 to 4.3 watts, with 5 dB gain and 35% typical power-added efficiency in the 9.2-10.2 GHz band. All three amplifier plots were made at about the 1 dB gain compression point; the drain current drawn under RF drive (quiescent current I_{DQ} = 10% I_{DSS}) was 45-50% I_{DSS}.

1 Watt and 2 Watt 15-Unit Performance

Figures 3 and 4 show the output power and power-added efficiency of 15 each of the 1 watt single-ended and 2 watt push-pull amps across the 9.2 - 10.2 GHz band. The retrofit of the high-Q capacitors in the 1 watt amplifiers increased their average mid-band efficiency by 5%, to 38%, and the gain improved .7 dB. At 9.7 GHz the standard deviations of the output power and efficiency were .29 dBm and 1.88% for the 1 watt single-ended lot and .22 dBm and 1.86% for the 2 watt push-pull lot.

Figures 5 and 6 give both output power and

the transmission phase shift (normalized to the small signal transmission phase) versus input power for the 1 and 2 watt groups. Note that the phase distortion is generally low until compression of the amps becomes significant, giving low AM/PM conversion at rated power. The high-Q capacitors also improved the 1 watt amplifier phase distortion characteristics.

Once the prototype tuning had been done on each type of amplifier, there was little or no tuning needed on any of the 30 units fabricated to obtain the consistency of performance exhibited in Figures 3 through 6. There were no extra or rejected amplifiers built.

Table I includes some typical values for other important parameters: 1) The noise figure for both amplifier types was approximately 2 dB lower at the 10% I_{DSS} bias point than at 50% I_{DSS}, implying less noise output from a class B amplifier when idle or driven by a small signal. 2) Third order intermodulation products are shown at output powers corresponding to approximately .5 dB gain compression. 3) The second harmonic content of the output signal was quite low, owing to the shorting effect of the drain bias stubs. The inherent phase cancellation properties of the push-pull amplifier at the second harmonic provided even more suppression; the -43 dBc level could be decreased to -60 dBc with slight tuning.

Table I. 1 and 2 Watt Amplifier Performance (9.6 GHz)

	1 Watt Unit	2 Watt Unit
AM-PM Conversion (max.)	1.6 deg/dB	3.0 deg/dB
Noise Figure (10% I_{DSS})	4.0 dB	5.6 dB
3rd Order Intermods.	-24 dBc	-16 dBc
2nd Harmonic Level	-35 dBc	-43 dBc

CONCLUSION

The results of this effort have demonstrated the high power-added efficiency obtainable in microwave FET power amplifiers by biasing at drain currents approaching pinchoff (10% I_{DSS} here) instead of the usual 50% I_{DSS} range. The high theoretical second harmonic content of this bias scheme was suppressed in the single-ended amplifier design with drain bias tuning and was lowered further by the push-pull topology. AM-to-PM conversion and third order intermodulation products were low, and the noise figure benefitted from the lower bias current.

A dual push-pull amplifier gave greater than 4.0 watts output, 35% power-added efficiency, and 5 dB gain in the 9.2 - 10.2 GHz band. Finally, the measured data for fifteen-lots of 1 and 2 watt amplifiers showed the repeatibility and consistency of performance needed for many amplifier applications.

REFERENCES

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2. R. G. Freitag, J. E. Degenford, and M. Cohn, "High Efficiency Single-Ended and Push-Pull Class B FET Power Amplifiers," presented at the 1985 GOMAC Conference, November, 1985.

ACKNOWLEDGEMENT

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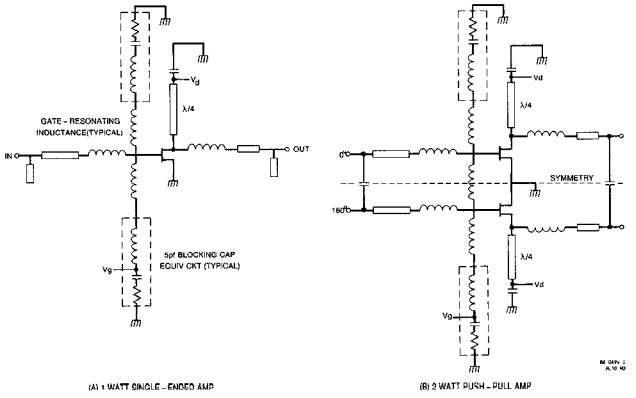


Figure 1

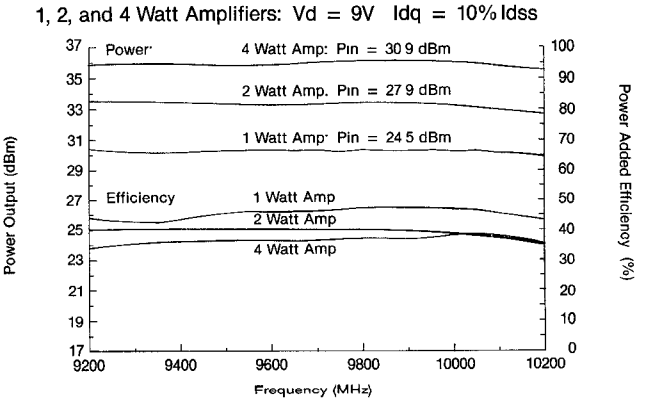
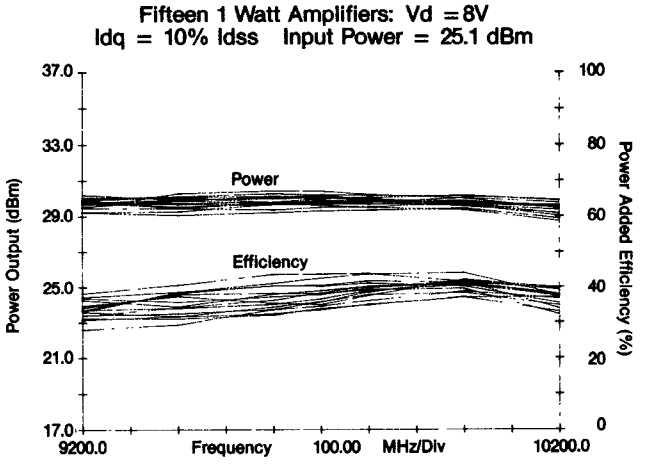


Figure 2



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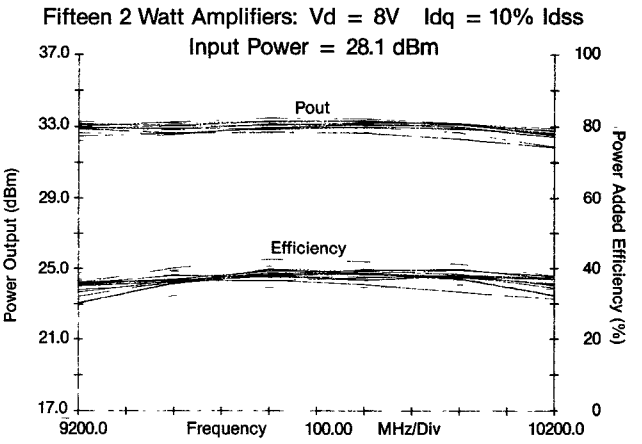

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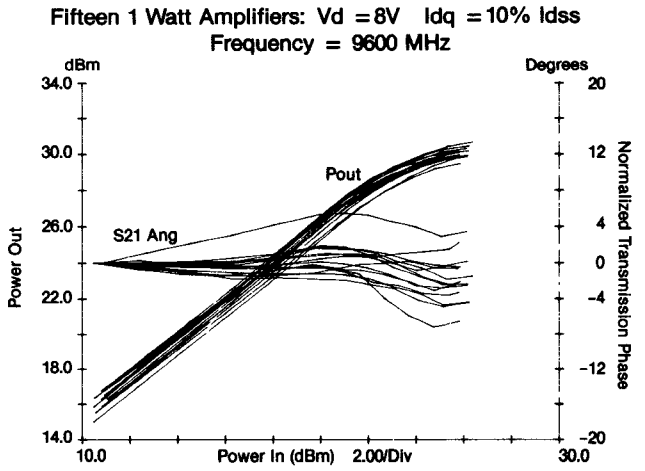

Figure 5

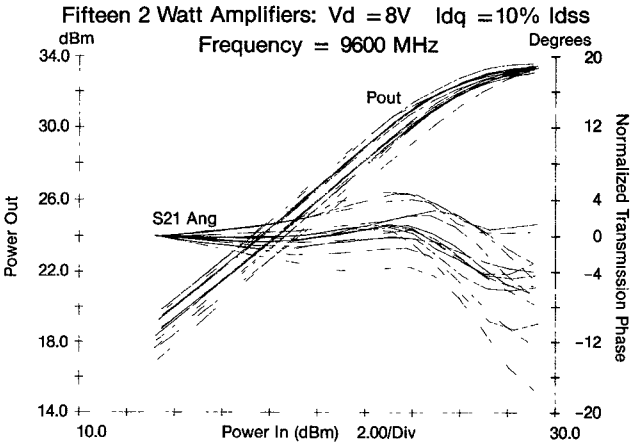

Figure 6